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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,376	02/20/2004	Georg Braun	1521.013705 (INFN/MB0062)	6404
46798 7590 10/08/2008 PATTERSON & SHERIDAN, LLP Gero McClellan / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056			EXAMINER PATEL, KAUSHIKKUMAR M	
			ART UNIT 2188	PAPER NUMBER
			MAIL DATE 10/08/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/783,376	Applicant(s) BRAUN ET AL.	
	Examiner Kaushikkumar Patel	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>4/24/2008</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed July 07, 2008 in response to PTO Office Action mailed April 04, 2008. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.

2. In response to last Office Action, claims 1, 16 and 22 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-22 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 16 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on April 24, 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 22 is rejected under 35 U.S.C. 101 the claimed invention is directed to non-statutory subject matter.

Claim 22 is directed towards a protocol, which is defined as “a set of conventions that governs the interactions of the processes, devices or other components within a system”. A set of conventions then is an abstract idea, per se and hence considered as non-statutory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grundy et al. (US 2004/0148482) in view of Pencis et al. (US 6,865,652) and Sakurai (US 5,959,930).

As per claims 1, 16 and 22 Grundy teaches a synchronous memory system/a method for communication/protocol (fig. 3), comprising:

a plurality of memory modules in a main memory (Grundy, fig. 3, items 107₁ - 107_{i+1}), with each memory module comprising at least two memory banks (Grundy, par.

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[0035], “the storage array 115 (which may include multiple storage arrays) being used for data storage”);

a memory control device configured to generate commands (Grundy, fig. 3, item 101, par. [0033], “the memory controller issues a data read command to a target memory device”).

Grundy fails to teach the commands comprise a plurality of command segments with respective plurality of elements, however Pencis teaches command comprises a plurality of command segments with respective plurality of elements (Pencis, col. 1, lines 55-57; col. 1, line 67 – col. 2, line 22). It would have been obvious to one having ordinary skill in the art at the time of the invention to use commands with command segments as taught by Pencis in the system of Grundy to provide narrow command bus (Pencis, col. 1, lines 55-57) thereby reducing space required to accommodate the bus lines on the integrated chip and/or board.

Grundy and Pencis combined teach wherein one of the command segments is a selection command segment for selecting at least two memory devices simultaneously, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment (Grundy, par. [0032] “each memory device in the chain is represented by a bit within a multi-bit device selection value, the bit being set if the corresponding memory device is part of the target group of memory devices”; abstract: “selects a set of two or more of the memory devices to be accessed”); and

a transfer bus for communication between the memory control device and the plurality of memory modules, wherein the transfer bus is in the form of a daisy chain

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structure and wherein the transfer bus comprises a plurality of parallel transfer lines (Grundy, fig. 3, par. [0037], "commands and data output from the memory controller 101 to the chain of memory devices 107 travel in one direction"; par. [0043], "the command line 156 and a set of N multi-purpose lines 158"); and wherein the memory control device is configured to transfer commands to the plurality of memory modules using the transfer bus (as explained above, commands and data output from the memory controller to the chain of memory devices, where it is inherent that the transfer bus transfers the commands), and wherein the transfer bus is configured to transfer the elements of a command segment in parallel over the parallel transfer lines (Grundy, par. [0044]), wherein the daisy chain structure comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of the memory module and a second point-to-point connection from the first memory module to the plurality of memory modules to a second memory module of the plurality of memory modules, whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain (Grundy, figs. 3 and 5A, pars. [0037], [0038]).

Grundy and Pencis combined teaches selecting two memory devices simultaneously as explained above but fail to teach selecting two memory banks from single memory device. Sakurai teaches selecting two memory banks simultaneously (Sakurai, abstract). Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to provide multi-bank selection method as taught by Sakurai in the system of Grundy and Pencis to improve read write operations faster (Sakurai, abstract).

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As per claims 2 and 17, Grundy teaches wherein each of the plurality of memory modules further comprises a buffer device for forwarding the commands to at least two memory banks in at least in at least one of a respective memory module of the plurality of memory modules and one or more other memory modules of the plurality of memory modules (Grundy, par. [0030]; "memory devices are chained to one another and to a memory controller via respective, high-speed, point-to-point signaling links", "commands and data received within a given memory device are retransmitted to a subsequent memory device in the chain after brief storage"; "each of the memory devices buffer incoming commands and data').

As per claims 3 and 18, Grundy and Sakurai teach wherein buffer device is configured to compare the bit pattern of a given selection command segment with one or more predetermined bit patterns and to determine whether the associated commands needs to be forwarded to at least one of: (i) the at least two memory banks in the respective memory module; (ii) and the one or more other memory modules (here it is noted that Grundy teaches buffering and forwarding commands (see claim 2 above), where it is readily apparent that there must be a logic to perform the comparison for respective bit pattern to determine whether the command is for the memory device or it needs to be forwarded to the next one and as noted above Sakurai teaches selecting multiple banks in the memory device means the command is forwarded to the at least two memory banks. see par. [0090] teaches command buffer).

As per claim 4, Grundy and Sakurai teach wherein the buffer device is configured to generate a chip select signal for the at least two memory banks (Grundy, par. [0032]; Sakurai, fig. 1, item 5).

Claim 19 is a combination of claims 3 and 4 thus claim 19 is rejected under same rationales as applied to claim 3 and 4 above.

As per claims 5 and 20, Grundy, Pencis, and Sakurai expressly fail to teach selection command segment is the first segment of the commands, however it is noted that without selection (e.g. chip/device select) command it is not possible to perform any memory operations and thus it would have been obvious to one having ordinary skill in the art at the time of the invention to send selection command segment first to select appropriate memory device to be read or written to.

As per claim 6, Grundy teaches wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system (Grundy, pars. [0043], [0049]).

As per claims 7 and 8, Grundy teaches wherein the commands for each memory bank contain an element for a clock enable signal for all the memory bank (Grundy, par. [0107]).

As per claims 9 and 10, Grundy teaches wherein the commands for each memory bank contain an element for an on-die termination signal for all the memory banks (Grundy, par. [0085]).

As per claim 11, Grundy teaches wherein the buffer device is designed to generate an on-die termination signal (Grundy, par. [0085]).

As per claim 12, Grundy teaches wherein commands contain an element for a reset signal (Grundy, par. [0068]).

As per claim 13, Grundy teaches a transfer line connecting the memory control device and at least one of the plurality of memory modules and configured to propagate a reset signal. As explained above with respect to claim 1, the bus propagates the signals to the memory device and as explained above with respect to claim 12, a reset signal is also propagated to the memory devices.

As per claim 14, Grundy and Sakurai teach wherein the commands contain an element for signaling that the command is intended for the buffer device. Here it is noted that as explained above with respect to claim 1, Grundy teaches sending commands to the first memory device and if necessary subsequently forwards the commands to the other memory devices in the chain, where it is readily apparent that the buffer device with selected memory device must determine whether the command is intended for the it self or the other memory device.

As per claims 15 and 21, Grundy teaches wherein the memory control device comprises a coding device for coding generated commands and the buffer control device comprises a decoding device for decoding received coded commands (Grundy, par. [0097]).

8. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greeff et al. (US 6,882,082) in view of Pencis et al. (US 6,865,652) and Joo (US 6,198,667).

As per claims 1, 16 and 22 Greeff teaches a synchronous memory system/a method for communication/protocol (fig. 1), comprising:

a plurality of memory modules in a main memory (Greeff, fig. 1, items 24, 26);

a memory control device configured to generate commands (Greeff, fig. 1, item 31, here it is noted that processor sends commands to memory controller, which in turn generates commands to memory devices).

Greeff fails to teach the commands comprise a plurality of command segments with respective plurality of elements, however Pencis teaches command comprises a plurality of command segments with respective plurality of elements (Pencis, col. 1, lines 55-57; col. 1, line 67 – col. 2, line 22). It would have been obvious to one having ordinary skill in the art at the time of the invention to use commands with command segments as taught by Pencis in the system of Greeff to provide narrow command bus (Pencis, col. 1, lines 55-57) thereby reducing space required to accommodate the bus lines on the integrated chip and/or board.

Greeff and Pencis failed to teach but in analogous art Joo teaches wherein memory device includes at least two memory banks and wherein one of the command segments is a selection command segment for selecting at least two memory banks simultaneously, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment (Joo, fig. 5, items XBANK1 and XBANK2, abstract). Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to select two memory banks simultaneously as taught by

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Joo in the system of Greeff and Pencis to decrease time required testing the memory (Joo, abstract).

Greeff, Pencis and Joo combined teach a transfer bus for communication between the memory control device and the plurality of memory modules, wherein the transfer bus is in the form of a daisy chain structure and wherein the transfer bus comprises a plurality of parallel transfer lines (Greeff, col. 3, lines 9-61); and wherein the memory control device is configured to transfer commands to the plurality of memory modules using the transfer bus (as explained above, commands and data output from the memory controller to the chain of memory devices, where it is inherent that the transfer bus transfers the commands), and wherein the transfer bus is configured to transfer the elements of a command segment in parallel over the parallel transfer lines (Greeff, col. 3, lines 32-48), wherein the daisy chain structure comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of the memory module and a second point-to-point connection from the first memory module to the plurality of memory modules to a second memory module of the plurality of memory modules, whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain (Greeff, fig. 1, col. 4, line 65 – col. 5, line 5; col. 6, lines 16-20; col. 7, lines 30-35).

As per claims 2 and 17, Greeff teaches wherein each of the plurality of memory modules further comprises a buffer device for forwarding the commands to at least two memory banks in at least in at least one of a respective memory module of the plurality of memory modules and one or more other memory modules of the plurality of memory

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modules (Greeff, col. 3, line 61 – col. 5, line 5, the interface circuit 30 buffers the commands and then forwards to the next memory device, although explicitly not shown, such buffer device is well known in the art).

As per claims 3 and 18, Greeff teaches wherein buffer device is configured to compare the bit pattern of a given selection command segment with one or more predetermined bit patterns and to determine whether the associated commands needs to be forwarded to at least one of: (i) the at least two memory banks in the respective memory module; (ii) and the one or more other memory modules (here it is noted that Greeff teaches buffering and forwarding commands (see claim 2 above), where it is readily apparent that there must be a logic to perform the comparison for respective bit pattern to determine whether the command is for the memory device or it needs to be forwarded to the next one and as noted above, Joo teaches selecting multiple banks in the memory device means the command is forwarded to the at least two memory banks).

As per claim 4, Greeff, Pencis and Joo teach selecting two memory banks simultaneously as taught above (claim 1), but expressly fail to teach wherein the buffer device is configured to generate a chip select signal for the at least two memory banks, however it is inherent in the system of Greeff, Pencis and Joo to generate a chip select signal for proper operation of the memory system.

Claim 19 is a combination of claims 3 and 4 thus claim 19 is rejected under same rationales as applied to claim 3 and 4 above.

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As per claims 5 and 20, Greeff, Pencis, and Joo expressly fail to teach selection command segment is the first segment of the commands, however it is noted that without selection (e.g. chip/device select) command it is not possible to perform any memory operations and thus it would have been obvious to one having ordinary skill in the art at the time of the invention to send selection command segment first to select appropriate memory device to be read or written to.

As per claim 6, Greeff teaches that the bus can have any number of parallel paths (Greeff, col. 3, lines 32-48), thus it can be inferred that that the number of transfer lines is a design choice, thus Greeff teaches wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system.

As per claims 7 and 8, Greeff teaches wherein the commands for each memory bank contain an element for a clock enable signal for all the memory bank (Greeff, col. 3, lines 33-40)

As per claims 9 and 10, Greeff teaches a terminator (col. 3, lines 25-28) but fails to teach an on-die termination signal for all the memory banks, however the technology for on-die terminator is well known in the art and the examiner takes official notice of the fact because on-die terminator eliminates the need for a terminator resistor to be associated with each line.

As per claim 11, Greeff teaches wherein the buffer device is designed to generate an on-die termination signal (As explained with respect to claims 9 and 10 above the having terminator requires generating the signal).

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As per claim 12, Greeff, Pencis and Joo explicitly fail to teach a reset signal, however memory devices are known to include reset signals and the examiner takes official notice of the fact because the reset signal is used to reset the memory device during initialization

As per claim 13, Greeff teaches a transfer line connecting the memory control device and at least one of the plurality of memory modules and configured to propagate a reset signal. As explained above with respect to claim 1, the bus propagates the signals to the memory device and as explained above with respect to claim 12, a reset signal is also propagated to the memory devices.

As per claim 14, Greeff, Pencis and Joo teach wherein the commands contain an element for signaling that the command is intended for the buffer device. Here it is noted that as explained above with respect to claim 1, Greeff teaches sending commands to the first memory device and if necessary subsequently forwards the commands to the other memory devices in the chain, where it is readily apparent that the buffer device with selected memory device must determine whether the command is intended for the it self or the other memory device.

As per claims 15 and 21, Greeff teaches wherein the memory control device comprises a coding device for coding generated commands and the buffer control device comprises a decoding device for decoding received coded commands (Greeff, fig. 2, item 47).

Conclusion

9. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

10. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Merritt (US 6,055,202) teaches a method of selecting multiple banks simultaneously.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is (571)272-5536. The examiner can normally be reached on 7.30 am - 4.00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
10/07/08

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